REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 4, 2002, and the references cited therewith.

Claims 70-76 are added; as a result, claims 62-76 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Forms, listing all references that were submitted with the Information Disclosure Statements filed on May 29, 2001, November 30, 2001, March 22, 2002, and May 7, 2002, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Double Patenting Rejection

Claim 62 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of U.S. Patent No. 6,143,636 (Attorney Docket no. 303.342US2). In addition, claim 62 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,238,976 B1 (attorney docket no. 303.330US2).

A Terminal Disclaimer in compliance with 37 C.F.R. 1.321(b)(iv) is enclosed herewith to overcome these rejections. The Terminal Disclaimer enclosed herewith disclaims both of the patents cited in the double patenting rejection. Accordingly, Applicant believes that the enclosed Terminal Disclaimer is sufficient to overcome both rejections. Applicant believes that the double patenting rejections are now moot, and respectfully requests that they be withdrawn.

New Claims

New claims 70-76 add no new matter, and are supported in the specification as follows:

Claim 70:

- Page 16, lines12-15 and page 20, lines 9-12 (forming first and second gate dielectric layers);
- Page 16, lines 15-16 and page 20, lines 12-13 (the first and second floating gate regions including a first conductive layer of N+ doped polysilicon);
- Page 18, lines 1-2 and page 21, lines15-18 (the first and second control gate regions including N+ doped polysilicon);
- Page 17, lines 24-26 and page 21, lines 15-18 (forming first and second gate lines);
- Page 18, lines 16-24 (removing material at intersecting portions of first troughs and second troughs).

Claim 71:

- Page 16, lines 15-16 and page 20, lines 12-13 (the first and second floating gate regions including a first conductive layer of N+ doped polysilicon).

Claim 72:

- Page 18, lines 1-2 and page 21, lines15-18 (the first and second control gate regions including N+ doped polysilicon).

Claim 73:

- Page 17, lines 24-26 and page 21, lines 15-18 (forming first and second gate lines).

Claim 74:

- Page 17, line 1 through page 18, lines 1-2, and page 21, lines15-18 (the first and second control gate regions formed together and including N+ doped polysilicon).

Claim 75:

- Page 18, lines 16-24 (removing material at intersecting portions of first troughs and second troughs).

Claim 76:

- Page 16, lines12-15 and page 20, lines 9-12 (forming first and second gate dielectric layers).

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6904) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date Jan. 30, 2003 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30th day of January, 2003.

Name Amy Moriarty

Signature Amy Moriarty